UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/210,540	12/14/1998	HAJIME NAKAYAMA	P982413	5288

26263 7590 11/19/2001

SONNENSCHEIN NATH & ROSENTHAL
P.O. BOX 061080
WACKER DRIVE STATION
CHICAGO, IL 60606-1080

EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/19/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/210,540	NAKAYAMA, HAJIME	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Upon further consideration, the final rejection in Paper No.7 is hereby withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **9 & 10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Claims **9 & 10** are incomplete because these claims depend on cancelled claim **2** withdrawn from further consideration.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5 Claims **1 & 3-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung (US 5,856,215) in view of Admitted prior art.

Regarding claims **1, 2, & 5**, Jung disclosures a semiconductor device comprising (Fig. 1):

a first element formation region (10) in which a device of a first conductivity type is formed; a second element formation region (20) separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed; a first gate

electrode (12) provided on said first element formation region and containing an impurity of the first conductivity type; a second gate electrode (22) provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type; a first impurity storage region (12') containing said first conductivity type impurity, having one end connected to an end of said first gate electrode; a second impurity storage region (22') containing said first conductivity type impurity, having one end connected to an end of said second gate electrode, wherein the first and second impurity storage region arranged in a direction different from the direction of arrangement of said first and second gate electrode.

Jung does not clearly show the gate electrodes 12 and 22 containing an impurity. However, it is acknowledged in the art that a p-type impurity is doped in the region of polycrystalline silicon interconnection layer for forming doped region in PMOS, while n-type impurity is doped in the region of polycrystalline silicon interconnection layer for forming doped region in NMOS. These doped regions are thereby made conductive and form gated electrode. This feature is inherent in Jung's device to provide the conductive gate electrode in CMOS device.

Jung also does not teach an impurity storage region. However, 12' and 22' would meet the broad recited limitations of "impurity storage region" because these regions hold impurity. The impurity storage region is just functional language. Thus, claimed structure is taken to be in the least obvious over Jung.

Jung does not teach the first and second impurity storage regions are physically connected to each other by a semiconductor layer. However, APA teaches in Fig.2

using a semiconductor layer to provide an electrical connection between PMOS and NMOS. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a semiconductor layer as taught by APA to provide electrical connection between gates of NMOS and PMOS in Jung's device. One of ordinary skill in the art would have recognized that the semiconductor layer and metal are an art recognized functional equivalent for providing electrical connection and therefore an obvious expedient.

Regarding claim **3**, Jung teaches the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

Regarding claim **4**, Jung teaches the first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second electrodes.

Regarding claim **5**, Jung teaches the first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

Regarding claim **9**, Jung teaches semiconductor layer be formed by polycrystalline silicon and first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

Regarding claim **10**, Jung teaches the width of said semiconductor layer physically connecting said first and second impurity storage regions are a value allowing

mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

Regarding claim **11**, Jung teaches the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes and the lengths of said first and second impurity storage regions are longer than said gate length.

6. Claims **6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung as modified by admitted prior art as applied to claim 1 as discussed above, and further in view of Joyner et al (US 6,114,741). The teaching of Jung as modified by admitted prior art has been discussed above.

Jung as modified by the admitted prior art does not teach element isolation region be buried in a trench formed a boundary between said first and second conductive type of element formation regions in a semiconductor substrate. However, Joyner et al teaches element isolation region (Fig. 1E) be buried in a trench formed a boundary between said first and second conductive type of element formation regions in a semiconductor substrate in order to isolate first and second conductive type regions.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use trench isolation in order to provide isolation between adjacent device regions.

Regarding claim **7**, Joyner et al teaches element isolation region isolates first and secon element formation region

Regarding claim **8**, Joyner et al teaches element isolation region is buried in a trench formed in semiconductor layers.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DHK
November 15, 2001

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800